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22903	7590 05/30/2006		EXAMINER		
COOLEY GODWARD LLP			MCCARTHY, CHRISTOPHER S		
	ENT GROUP EN BUILDING		ART UNIT	PAPER NUMBER	
875 15TH STREET, N.W. SUITE 800			2113		
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Please find below and/or attached an Office communication concerning this application or proceeding.

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		Application No.	Applicant(s)	
		09/844,669	THEKKATH, RADHIKA	
	Office Action Summary	Examiner	Art Unit	
		Christopher S. McCarthy	2113	
Period fo	The MAILING DATE of this communication app or Reply	ears on the cover sheet with the c	orrespondence address	
A SH WHIC - Exte after - If NC - Failu Any	ORTENED STATUTORY PERIOD FOR REPLY CHEVER IS LONGER, FROM THE MAILING DANSIONS of time may be available under the provisions of 37 CFR 1.13 SIX (6) MONTHS from the mailing date of this communication. o period for reply is specified above, the maximum statutory period we are to reply within the set or extended period for reply will, by statute, reply received by the Office later than three months after the mailing ed patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be tin will apply and will expire SIX (6) MONTHS from the cause the application to become ABANDONE	N. nely filed the mailing date of this communication. (D (35 U.S.C. § 133).	
Status				
2a)□	Responsive to communication(s) filed on <u>06 Ap</u> This action is FINAL. 2b) This Since this application is in condition for allowar closed in accordance with the practice under E	action is non-final.  nce except for formal matters, pro		
Dispositi	ion of Claims			
5)□ 6)⊠ 7)⊠	Claim(s) 1-21 is/are pending in the application.  4a) Of the above claim(s) is/are withdray  Claim(s) is/are allowed.  Claim(s) 1-13 and 15-21 is/are rejected.  Claim(s) 14 and 15 is/are objected to.  Claim(s) are subject to restriction and/or	vn from consideration.		
Applicat	ion Papers			
10)🖾	The specification is objected to by the Examine The drawing(s) filed on <u>30 April 2001</u> is/are: a) Applicant may not request that any objection to the Replacement drawing sheet(s) including the correct The oath or declaration is objected to by the Ex	☑ accepted or b) ☐ objected to drawing(s) be held in abeyance. Sertion is required if the drawing(s) is object.	e 37 CFR 1.85(a). ijected to. See 37 CFR 1.121(d).	
Priority (	under 35 U.S.C. § 119			
а)	Acknowledgment is made of a claim for foreign  All b) Some * c) None of:  1. Certified copies of the priority documents  2. Certified copies of the priority documents  3. Copies of the certified copies of the priority application from the International Bureau  See the attached detailed Office action for a list	s have been received. s have been received in Applicati rity documents have been receive u (PCT Rule 17.2(a)).	ion No ed in this National Stage	
	ce of References Cited (PTO-892)	4) 🔲 Interview Summary		
2) Notice 3) Information	ce of Draftsperson's Patent Drawing Review (PTO-948) mation Disclosure Statement(s) (PTO-1449 or PTO/SB/08) er No(s)/Mail Date <u>1-4</u> .	Paper No(s)/Mail D		

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#### **DETAILED ACTION**

#### Claim Rejections - 35 USC § 101

1. Claims 19-20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claim 19 cites a "computer data signal embodied in a transmission medium". Signals contained on a transmission medium are currently deemed as non-statutory as being non-tangible. Claim 20 cites program code, but not stored on a tangible medium. Program code not stored on a tangible medium is deemed non-statutory.

## Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 3. Claims 1,2, 4-7, and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Anderson et al. U.S. Patent 5,918,004.

As per claim 1, Anderson teaches a tracing control method, comprising of initiating tracing of data during execution of a program that includes a plurality of instructions, said tracing initiation being based on a first trace control command embodied in one or more instructions of said program (column 4, lines 41-42); and halting said tracing based upon a second trace control

command embodied in one or more instructions of said programs wherein said first trace control command and said second trace control command are operative to trigger tracing on and off without using one or more breakpoints (column 5, lines 17-21, wherein, no breakpoints are used).

As per claim 2, Anderson teaches the tracing control method of claim 1, wherein said first trace control command generates a trace enable indication and said second trace control command generates a trace disable indication (column 5, lines 17-21, wherein, the citation is equivalent to the on/off state of Anderson).

As per claim 4, Anderson teaches the tracing control method of claim 2, wherein said first trace control command is inserted in an entry point to a section of code, and said second trace control command is inserted in an exit point to said section of code (column 5, lines 17-21; column 4, lines 41-47).

As per claim 5, Anderson teaches the tracing control method of claim 1, wherein said first trace control command and said second trace control command are included within said program prior to execution of said program (column 4, lines 41-47).

As per claim 6, Anderson teaches a method for tracing a section of program code, comprising executing a program that includes a plurality of instructions, said plurality of instructions including one or more trace control commands (column 4, liens 41-47), initiating tracing of data upon entering a section of code in said program, said tracing initiation being based on a first trace control command in said program; and halting said tracing upon leaving a section of code in said program, said halting being based upon a second trace control command in said programs (column 5, lines 17-21); wherein said first trace control command and said

second trace control command are operative to trigger tracing on and off without using one or more breakpoints (column 5, lines 17-21).

As per claim 7, Anderson teaches the method of claim wherein said first trace generates a trace enable indication and said second trace control command disable indication. control command generates a trace (column 5, lines 17-21).

As per claim 9, Anderson teaches the tracing control method of claim 6, wherein said first trace control command and said second trace control command are included within said program prior to execution of said program (column 5, lines 17-21; column 4, lines 41-47)).

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
- 5. Claims 10-13, 16-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Watanabe U.S. Patent Application Publication US2001/0054175.

As per claim 10, Watanabe teaches a tracing system, comprising an embedded processor, said embedded processor including, a processor core for executing instructions (paragraph 0025); and trace generation logic that is operative to generate trace data for said instructions executing in said processor core, said trace generation logic capable of being controlled by hardware input signals (paragraphs 0027, 0029) and by a software-settable trace control register adapted to be set by at least one trace control command embodied in instructions of a program to be traced

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(paragraph 0026); wherein said tracing system is operative to utilize said at least one trace control command to trigger tracing on and off without requiring the use of one or more breakpoints (paragraph 0027).

As per claim 11, Watanabe teaches the tracing system of claim 10, wherein said embedded processor further includes a trace capture block that receives trace data from said trace generation logic (paragraph 0027).

As per claim 12, Watanabe teaches the tracing system of claim 11, wherein said trace capture block sends trace data to an off-chip trace memory (paragraph 0027, 0028).

As per claim 13, Watanabe teaches the tracing system of claim 11, wherein said hardware input signals are received by said trace generation logic from said trace capture block (paragraph 0027).

As per claim 16, Watanabe teaches the tracing system of claim 10, wherein said softwaresettable trace control register is set by trace control commands that are embodied in one or more instructions of a program (paragraph 0040, 0042).

As per claim 17, Watanabe teaches the tracing system of claim 16, wherein said trace control commands are included within said program prior to execution of said program (paragraph 0026).

As per claim 18, Watanabe teaches a computer program product comprising: computerreadable program code for causing a computer to describe an embedded processor, said embedded processor including a processor core for executing instructions (paragraph 0025), and trace generation logic that is operative to generate trace data for said instructions executing in said processor core, said trace generation logic capable of being controlled by hardware input

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signals (paragraph 0027, 0029) and by a software-settable trace control register adapted to be set by at least one trace control command embodied in instructions of a program to be traced (paragraph 0026); and a computer-usable medium configured to store the computer-readable program codes; wherein said embedded processor is operative to utilize said at least one trace control command to trigger tracing on and off without requiring the use of one or more breakpoints (paragraph 0027).

As per claim 19, Watanabe teaches a computer data signal embodied in a transmission medium comprising computer-readable program code for causing a computer to describe an embedded processor, said embedded processor including a processor core for executing instructions (paragraph 0025), and trace generation logic that is operative to generate trace data for said instructions executing in said processor core, said trace generation logic capable of being controlled by hardware input signals (paragraph 0027, 0029) and by a software-settable trace control register adapted to be set by at least one trace control command embodied in instructions of a program to be traced (paragraph 0026); wherein said embedded processor is operative to utilize said at least one trace control command to trigger tracing on and off without requiring the use of one or more breakpoints (paragraph 0027).

As per claim 20, Watanabe teaches a method for enabling a computer to generate a tracing system, comprising transmitting computer-readable program code to a computer, said computer-readable program code including computer-readable program code for causing a computer to describe an embedded processor, said embedded processor including a processor core for executing instructions (paragraph 0025), and trace generation logic that is operative to generate trace data for said instructions executing in said processor core, said trace generation

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logic capable of being controlled by hardware input signals (paragraphs 0027, 0029) and by a software-settable trace control register adapted to be set by at least one trace control command embodied in instructions of a program to be traced (paragraph 0026); wherein said embedded processor is operative to utilize said at least one trace control command to trigger tracing on and off without requiring the use of one or more breakpoints (paragraph 0027).

# Claim Rejections - 35 USC § 103

- 6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
  - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 7. Claims 3, 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson in view of *The Authoritative Dictionary of IEEE Standards Terms* (referred to hereon as IEEE).

As per claim 3, Anderson teaches the tracing control method of claim 2, wherein a trace control indication is embodied in a field of a trace control memory that is written to upon execution of a trace control command (column 7, lines 23-25). Anderson does not explicitly teach wherein the memory is a register. IEEE teaches a register (page 949). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the register of IEEE as the memory of Anderson. One of ordinary skill in the art would have been motivated to use the register of IEEE as the memory of Anderson because IEEE teaches using a register for the purpose of a device capable of retaining information; this is an explicit desire of Anderson.

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As per claim 8, Anderson teaches the tracing control method of claim 7, wherein a trace control indication is embodied in a field of a trace control memory that is written to upon execution of a trace control command (column 7, lines 23-25). Anderson does not explicitly teach wherein the memory is a register. IEEE teaches a register (page 949). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the register of IEEE as the memory of Anderson. One of ordinary skill in the art would have been motivated to use the register of IEEE as the memory of Anderson because IEEE teaches using a register for the purpose of a device capable of retaining information; this is an explicit desire of Anderson.

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8. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe in view of House et al. U.S. Patent 6,119,247.

As per claim 21, Watanabe teaches the method of claim 20. Watanabe does not teach wherein computer-readable program code is transmitted to said computer over the Internet.

House does teach code transmitted to a computer over the Internet (abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the Internet transmission process of House in the process of Watanabe. One of ordinary skill in the art would have been motivated to use the Internet transmission process of House in the process of Watanabe because House teaches a programming development environment that supports development of applications; and explicit desire of Watanabe (paragraph 0022).

Allowable Subject Matter

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9. Claims 14-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

#### Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached PTO-892.

### Response to Arguments

11. Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher S. McCarthy whose telephone number is (571)272-3651. The examiner can normally be reached on M-F, 9 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher S. McCarthy

Examiner Art Unit 2113

csm